August 13, 2025

Dr. Afshan Amin Khan

HEADING	Educator with Real-World ASIC Tape-Out Experience. I possess the relevant experience 5+ years of teaching and additionally experience of working on tools like Innovus, Static Timing Analysis tools Tempus, and Physical Verification tool Calibre. Moreover, I have comprehensive understanding of the full ASIC flow from RTL to GDSII, with a successful tape-out in collaboration with SCL Chandigarh and CDAC Bengaluru.

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HIGHEST QUALIFICATION — Ph.D in Engineering from National Institute of Technology,Srinagar,JandK,India 190006.

PRESENT EMPLOYMENT — Working as Manager-VLSI at Futurense Technologies PVT LTD, holding the key responsibility of development and management of VLSI courses, while ensuring alignment with VLSI and AI industry standards. Analyze course feedback and performance metrics to continuously improve course offerings and ensure high-quality educational experiences in VLSI and AI related courses.

RECENT ACTIVITY — Recently completed the RTL to GDSII design of an ASIC under the project titled "ASIC Design of Arbitration Unit for NoC", funded by MeitY, Govt. of India. I worked as the VLSI designer for the project. The tools that I have used mainly include Vivado IDE, Cadence(nclaunch,Inovous,Virtuoso), Calibre from Mentor Graphics. The chip was fabricated in collaboration with Chip Centre, C-DAC, Bengaluru. The fabricated ASIC has been received successfully.

SUMMARY — With a robust grounding in VLSI and Network on Chip (NoC), my PhD from NIT Srinagar has been focused on advancing digital IC design and fostering innovative research. At the University of Kashmir, my role as a Lecturer honed these competencies, enabling me to contribute significantly to academia.

My work at Islamic University involves developing design specifications that underpin the next wave of technological advancements. The expertise honed through my PhD, coupled with a practical approach to education, drives my mission to equip students with cutting-edge skills and a deep understanding of VLSI and NoC, preparing them for the demands of the industry.

INTERESTS — VLSI Design, Low power Digital IC design, ASIC Design, Scheduling for NoC.

EDUCATION

Islamic University of Science and Technology, Awantipora, JK, India. — July 2007 – 2011
B.Tech — (Percentage 84.31)

Lovely Professional University, Punjab, JK, India. — August 2012 – July 2014
M-Tech — (Percentage 70.74)

National Institute of Technoloy, Srinagar, JK, India — Dec 2015 – Feb 2022
PhD — (Percentage 8.70)

Fellowship Received fellowship under Visvesvaraya PhD scheme, MeitY, Govt. of India, for pursuing PhD.

National Level Examinations
Qualified GATE-2016
Qualified UGC NET-2015

Professional Training/Courses
-3-day 27th international Seminar on "VLSI Design," held at **Indian Institute of Technology Bombay (IITB)** from 5th to 10th Jan 2014.
-10-day workshop on "Xilinx Tools" organized by **Indian Institute of Sciences, Bangalore, sponsored by SMDP-C2SD program, Ministry of Electronics and Information Technology, GOI., 2016**
-1-Month visit to **CDAC Bangalore** for final tailoring and submission of the ASIC of an arbiter unit,2019.
- 5- Days Training Workshop on "VLSI to System Design: Silicon to End Application Approach" organized by **All India Council for Technical Education in collaboration with Arm Education and STMicrcoelectronics**, from 31 July to 4 August 2023.

Courses Taught VLSI Design, Digital Signal Processing, HDL Design, Digital Design, Communication Systems & VLSI Design Lab.

Technical Skills
Simulation tools and skills: CADENCE, Clock synthesis, lint CDC, RTL to GDSII, Physical design, Pad ring creation and wire bonding diagram, Xilinx Vivado, Advanced design systems (ADS).
Programming: C, Verilog, VHDL for FPGA platforms.
Research Document typesetting : Latex
Applications: MS Word, MS Excel, MS Power Point
Platforms: Windows, Linux.

Experience
-Kashmir University, Srinagar, JK, India. 23-04-2014 to 15-01-2015
Lecturer
-NIT, Srinagar, JK, India. 13-03-2015 to 23-12-2015
Assistant Professor
-IOT Zakura , Kashmir University, Srinagar, JK, India. 02-04-2021 to 26-02-2023
Lecturer
-Islamic University of Sc. and Tech., Awantipora, JK, India. 27-02-2023 to 01-10-2023
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Publications Journals and Conferences

- "A Review Paper On 3-T Xor Cells And 8-T Adder Design in Cadence180nm," in proceedings of International Conference on Convergence of Technology (I2CT) – IEEE, Pune, India-2014.
- "Comparative Analysis of Carry Select Adder using 8T and 10T Full Adder Cells," in the proceedings of International Conference on Communication and Signal Processing(ICCSP), Tamil Nadu, India-2014.
- "Performance Analysis of CSA using BEC and FZF Logic with Optimized Full Adder Cell," in the proceedings of International Conference On Computing & Communication Technologies (ICCCT), IEEE, Hyderabad, India-2014.
- "Comparative Analysis Of Full Adder Cells in Nano-scale For Cascaded Applications," in proceedings of International Conference On Advances In Computers, Communication and Electronic Engineering (COMMUNE), Department of electronics and Instrumentation, University of Kashmir 2015.

- “Buffer aware arbiter design to achieve improved QoS for NoC,” in proceedings of TENCON 2017 - IEEE Region 10 Conference, Penang, Malaysia, 2017.
- “Fault-Tolerant Buffer Aware Round Robin Arbiter Design for NoC Architectures” in International Journal of Computing and Digital Systems, ISSN (2210-142X), Issue 8, Vol No.3-May-2019, http://dx.doi.org/10.12785/ijcds/080307
- “Applicability of mobile contact tracing in fighting pandemic (COVID-19): Issues, challenges and solutions” in Computer Science Review Volume 38, November 2020, 100307, https://doi.org/10.1016/j.cosrev.2020.100307
- ”Adaptive hybrid arbiter design for real-time traffic-aware scheduling.” In Journal of Circuit World,2021. https://doi.org/10.1108/CW-10-2020-0268
- ”Scheduling Strategies and Future Directions For Noc: A Systematic Literature Review” In Journal of Automatic Control and Computer Sciences,2023, Vol. 57, No. 4, pp. 413–421. https://10.3103/S0146411623040041
- ”Design of Efficient Low-cost Ventilator for Emergency COVID19 Patients ” In Indian Science, Technology and innovation for COVID-19 Research. https://www.indiascienceandtechnology.gov.in/node/124261
- Granted patent titled ”INDUCTION CLOTH IRON MACHINE” bearing design number 402754-001

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ISSN 0146-4116, Automatic Control and Computer Sciences, 2023, Vol. 57, No. 4, pp. 413–421.

Scheduling Strategies and Future Directions for NoC: A Systematic Literature Review

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Received August 4, 2022; revised October 24, 2022; accepted November 11, 2022

Abstract—Network on chip interconnection technology is emerging as a viable solution for the replacement of the traditional interconnection techniques. The efficiency of a system typically depends upon the efficiency of its internal blocks. One such building block of a NoC is a scheduling unit, which performs the critical job of scheduling the movement of the packets in a NoC. A Scheduler has a close relationship with the efficiency of the NoC router in particular and the over-all NoC in general. Therefore, an in-depth study of the literature available on scheduling for NoC is of prime importance. In this work, we conduct a systematic literature review of scheduling strategies discussed in various literature. The primary goal of this research is to provide a thorough understanding of various scheduling strategies, thereby assisting a designer in determining the best scheduling strategy for the intended applications. Moreover, we highlight various performance parameters that determine the performance of a scheduler. As a conclusion, from the studies considered for review, we compiled a list of various tools and resources used and developed by research community for analysis and design of schedulers and NoCs. The different databases that were evaluated for the collection of the studies published include Science Direct, Springer Link, ACM Digital Library, IEEE Xplore, Wiley Online, and MDPI.

Keywords: adaptive scheduler, NoC arbiter, NoC scheduler, scheduling, arbitration, NoC optimization, NoC implementation resources, NoC implementation tools

DOI: 10.3103/S0146411623040041

1. INTRODUCTION

Moore's law brings forth the fact that the number of transistors in an integrated circuit (IC) increases by two folds every 18 months. Moore's law is expected to become irrelevant at any time. It still holds well, however, thanks to the advent of the latest methodologies of system design that embed many cores in a given space. The advent of multiprocessor system-on-chip (MP SoC) and many-core devices has led to the implantation of a greater number of devices on a single die, resulting in a tremendous increase in the number of interconnected devices on a single die of silicon. It becomes evident now that the communication between these interconnected modules needs to be handled by a sophisticated interconnection fabric. A traditional approach to connect these systems on a single die was the deployment of a point-to-point interconnection fabric, or a common bus of interconnection wires. A major drawback of such interconnection technologies is that they are not scalable, especially considering the latest trend of field programmable system-on-chip (FPSoC). Traditional interconnection techniques do not meet the performance and power requirements of a design. Thus, a new design paradigm such as network on chip (NoC) needs to be cautiously studied and improved for such systems.

An efficient and reliable NoC is expected to overcome the limitations of the previous interconnection methods. Since a NoC is an interconnection module that uses data packets as a source of communication between the modules of a high-density system [1]. It is a well-known fact that in order to devise an efficient NoC, a basic design approach is to study the possibilities of improvement in the efficiency of its basic building blocks. While analyzing a NoC, it is clear that a router is its basic component, which is repeated *n* number of times to form a network. The internal blocks of a router can be broadly adhered to either the data path or the control path of a router. Considering the fact that the latency attached to the data path of a router is actually a function of the time taken by the data to arrive from the previous nodes, it ultimately depends upon the components along the control path of a router that determine the final latency of the

Adaptive hybrid arbiter design for real-time traffic-aware scheduling

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Abstract

Purpose – This work focused on a basic building block of an allocation unit that carries out the critical job of deciding between the conflicting requests, i.e. an arbiter unit. The purpose of this work is to implement an improved hybrid arbiter while harnessing the basic advantages of a matrix arbiter.

Design/methodology/approach – The basic approach of the design methodology involves the extraction of traffic information from buffer signals of each port. As the traffic arrives in the buffer of respective ports, information from these buffers acts as a source of differentiation between the ports receiving low traffic rates and ports receiving high traffic rates. A logic circuit is devised that enables an arbiter to dynamically assign priorities to different ports based on the information from buffers. For implementation and verification of the proposed design, a two-stage approach was used. Stage I comprises comparing the proposed arbiter with other arbiters in the literature using Vivado integrated design environment platform. Stage II demonstrates the implementation of the proposed design in Cadence design environment for application-specific integrated chip level implementation. By using such a strategy, this study aims to have a special focus on the feasibility of the design for very large-scale integration implementation.

Findings – According to the simulation results, the proposed hybrid arbiter maintains the advantage of a basic matrix arbiter and also possesses the additional feature of fault-tolerant traffic awareness. These features for a hybrid arbiter are achieved with a 19% increase in throughput, a 1.5% decrease in delay and a 19% area increase in comparison to a conventional matrix arbiter.

Originality/value – This paper proposes a traffic-aware mechanism that increases the throughput of an arbiter unit with some area trade-off. The key feature of this hybrid arbiter is that it can assign priorities to the requesting ports based upon the real-time traffic requirements of each port. As a result of this, the arbiter is dynamically able to make arbitration decisions. Now because buffer information is valuable in winning the priority, the presence of a fault-tolerant policy ensures that none of the priority is assigned falsely to a requesting port. By this, wastage of arbitration cycles is avoided and an increase in throughput is also achieved.

Keywords Circuit implementation, Circuit simulation, Circuit networks, Fair arbiter, Hybrid arbiter, Traffic aware, Adaptive matrix arbiter, Fault tolerance, NoC arbiters, Buffer aware

Paper type Research paper

1. Introduction

The emphasis on miniaturization of the devices has led researchers toward new vision for system design and implementation, which leads the current very large-scale integration (*VLSI*) design industry toward adoption of highly scaled-down devices for system implementation. By the use of micro-fabrication and other technologies, possibilities of developing reliable lab on chip are ever growing (Bogue, 2016). Latest solutions for miniaturization are also evolving such as use of nanomagnetic logic (Farzaneh *et al.*, 2020). Embedding scaled-down device inside a chip has always been a challenge for the system designers. As a result of taking up these challenges, researchers have come up with the development of efficient and sophisticated system-on-chip (SoC) and multiprocessor system-on-chip (MP-SoC) architectures. Low power and area-efficient system design techniques incorporated with these systems are expected to revolutionize the way we think about digital systems (Wolf *et al.*, 2008; Khan and Mir, 2017; Khan and Mir, 2019; Sabu and Batri, 2020). However, traditional approach of interconnection of modules inside these complex systems is not feasible. Primarily, because of the increased parasitic effects caused by high wiring complexity and higher operating frequency requirements of these systems (Sharma *et al.*, 2011). NoC is expected to play a vital role in providing high-performance communication in SoC and MPSoC systems (Rowlands and Philip, 2019). To harness more benefits by using such technologies, use of through silicon via technology for fabrication is also a viable solution (Lau, 2011). Because of the advent of such

The current issue and full text archive of this journal is available on Emerald Insight at: **https://www.emerald.com/insight/0305-6120.htm**

Circuit World
© Emerald Publishing Limited [ISSN 0305-6120]
[DOI 10.1108/CW-10-2020-0268]

This publication is an outcome of the R&D work undertaken project supported by Visvesvaraya PhD Scheme, Ministry of Electronics & Information Technology, Government of India bearing unique awardee number MEITY-PHD-2020.

Received 1 October 2020
Revised 14 December 2020
Accepted 21 January 2021

Computer Science Review 38 (2020) 100307

Contents lists available at ScienceDirect

Computer Science Review

journal homepage: www.elsevier.com/locate/cosrev

Review article

Applicability of mobile contact tracing in fighting pandemic (COVID-19): Issues, challenges and solutions

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ARTICLE INFO

Article history:
Received 1 May 2020
Received in revised form 26 July 2020
Accepted 17 September 2020
Available online 23 September 2020

Keywords:
COVID-19
Contact tracing
Security
Privacy
Scalability

ABSTRACT

Contact Tracing is considered as the first and the most effective step towards containing an outbreak, as resources for mass testing and large quantity of vaccines are highly unlikely available for immediate utilization. Effective contact tracing can allow societies to reopen from lock-down even before availability of vaccines. The objective of mobile contact tracing is to speed up the manual interview based contact tracing process for containing an outbreak efficiently and quickly. In this article, we throw light on some of the issues and challenges pertaining to the adoption of mobile contact tracing solutions for fighting COVID-19. In essence, we proposed an Evaluation framework for mobile contact tracing solutions to determine their usability, feasibility, scalability and effectiveness. We evaluate some of the already proposed contact tracing solutions in light of our proposed framework. Furthermore, we present possible attacks that can be launched against contact tracing solutions along with their necessary countermeasures to thwart any possibility of such attacks.

Contents

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https://doi.org/10.1016/j.cosrev.2020.100307

International Journal of Computing and Digital Systems
ISSN (2210-142X)
Int. J. Com. Dig. Sys. 8, No.3 (May-2019)
http://dx.doi.org/10.12785/ijcds/080307

Fault-Tolerant Buffer Aware Round Robin Arbiter Design for NoC Architectures

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Abstract: An arbiter is identified as one of the critical components of the NoC router. Among various arbitration schemes, Round-Robin arbiter is one among the popular arbitration schemes. In this work we have proposed an arbitration scheme that will be able to solve the problem of constant wait time of a conventional Round-Robin arbiter and will provided some additional features as well. The superiority of the proposed design is its ability to overcome this constant wait time, by identifying the real-time requirements of each port, based on information from respective buffers. The additional feature of the proposed algorithm is its fault-tolerant behavior for the errors related to buffer information. The proposed design is implemented using Vivado IDE and is verified on Zed-board Zynq-7000 FPGA platform. Simulation results reveal that the proposed algorithm has completely eradicated the drawback of constant wait time by performing arbitration dynamically. More importantly, it was observed that the proposed algorithm is tolerant to any temporary or permanent fault for deciding priorities. These major improvements in a Conventional round robin arbiter are achieved at the cost of 36% increase in area and a bonus 8% and 2% improvement in delay and operating frequency respectively.

Keywords: Fault Tolerant, Round Robin arbitration, Starvation Free, Buffer Aware, MPSoC, SoC, High Throughput

1. Introduction

The constant trend of decrease in the transistor feature size has opened new doors of research and analysis for the modern-day technocrats, such that more research efforts are intended towards the development of innovative and effective methods to overcome the unwanted effects arising due to decrease in transistor feature size. More importantly as the possibility of increasing the density of devices on the die has become higher, new avenues of developing efficient system architectures such as System on Chip (SOC) and Multiprocessor System on Chip (MPSOC) based systems have come to the picture. Modern day electronic system design has been revolutionized by the introduction of MPSoC paradigm [1, 2].Observing the growing number of cores on a single die, where these cores are expected to generate a large set of communication data, there is an immense need to connect them with specialized communication hardware. Realizing the needs of these systems, a feasible, high performance, reusable and scalable Thus Network on Chip (NOC) can be a promising solution [3]. The use of a communication network implemented together on a single die alongside the processing core can be a sophisticated and natural solution [4]. Thus, in near future, we can expect that MPSOCs or SOCs will be designed with integrated network on chip architectures. One such expected architecture is shown in figure 1. It depicts a 2D 8X8 Mesh topology, where each core tile is capable enough to process data and later forward this processed data to the desired location using the dedicated communication module associated with the core. Many such dedicated communication modules will form a network housed on to the chip, known as Network-on-Chip. A router, seemingly small but in itself is a complete system having various sub-modules. It is implied that now the speed, area and power of the network will depend upon the router as a basic unit [2].Thus, efficient implementation of internal modules of a router is of prime importance for achieving a high-performance router and ultimately a NoC fabric. An efficient arbitration unit is key to the performance of a high-speed switch or a router [5].The use of an effective arbitration scheme can affect the network performance [4]. Thus an efficient and reliable arbitration between the sources and destination becomes a major design concern. A significant problem in an arbiter design is its low-cost implementation, where cost relates to the amount of delay, area and other performance parameters as well[6].Typically, an ideal arbiter is expected to exhibit fairness, mutually

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Buffer Aware Arbiter Design to Achieve Improved QoS for NoC

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***Abstract*—In order to meet the need for high-speed data processing, system designers have adopted Multi-Processor System-on-Chip (MPSoC) design. Network-on-chip (NoC) promises to be a viable solution as the basic communication fabric for such designs. A router is the basic component of NoC and using efficient internal blocks to design a router is expected to improve the performance of a router as a whole. One such block of prime importance is an arbitration unit. The commonly used arbitration logics include Fixed Priority, Lottery and Round Robin algorithm. However, they lack the capability of dynamically changing the priority according to data flit rates of specific ports. Thus a requester sending more requests can suffer from starvation and ultimately loss of data if not served within due course of time. In this work, we propose an improved Round Robin algorithm, for increasing Quality-of-Service (QoS) of a router. This is achieved by making use of an additional control signal from the buffer of each input port named as Buffer full (b_f). This addition will help us avoid the starvation condition of input ports which have more data flits to send than the lightly loaded input ports. The superiority of the proposed method than the conventional one is its feasibility for non-uniform traffic applications. All the circuits are implemented using Vivado 2016.2, with Zed-board as the target board. The proposed design is expected to find its application in areas where the traffic pattern is not certain and can vary from uniform to hot-spot traffic.**

Keywords—Quality of Service, Round Robin algorithm, starvation, Buffer status, Real Time Application, SoC.

I. Introduction

One of the major challenges for the next generation designers is to build a cost effective and time effective approach for system design, so as to meet the technological zenith requirements of the market. However a typical feature of all market needs is high processing power, so as to boost the processing speed of a system. This requirement was traditionally met by increasing the clocking frequency of the cores involved, however due to decrease in the feature size of the devices, static power consumption has been added as a design constraint of a certain fabricated area. Thus by using high clocking frequency of the modules used, overall power consumption is expected to increase by a great deal. This has put a limit on further increase of clocking frequency of modules used. Another approach of increasing processing power of a system can be achieved by increasing the number of systems on a chip, such that the task is now distributed between the modules. This system design approach is called as System on Chip (SoC) design methodology. SoC is expected to have many modules on a single die, which can be similar or different in their role to the overall system. Once a system is developed using SoC design methodology, it becomes evident that the system will generate huge amount of communication data, so as to communicate and synchronize between the modules. Hence it becomes a primary concern for the designers to design a communication fabric that is fast, reliable and consistent. Now, it will not only be important that how fast a particular element processes data but also how fast the processed data is clubbed together and sent to the outside world for further usage. Replacing systems on a single die with processors we then have many processing cores on a single die, which distribute the unprocessed data between them and eventually return back the processed data to the desired destination. This approach of system design is called as MPSoC design. Electronic system design is being revolutionized by the widespread adoption of the MPSoC paradigm [1]. Traditionally, a SoC or an MPSoC system, interconnects intellectual properties (IP) by use of a bus-based interconnect system. However when the number of participating components is more, then the bus system will have

Performance Analysis of CSA using BEC and FZF Logic with Optimized Full Adder Cell

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Abstract— **This paper shows the implementation and comparison of Carry Select Adder (CSA) using BEC (Binary Excess one Converter) and First Zero Finding (FZF) logic implementation techniques with optimization of the Full Adder (FA) cell by minimize number of transistors. The results have been analyzed and compared for implementation of both the above logic styles for 28T, 10T and 8T FA cells where as keeping all other basic cells used for implementation of BEC and FZF based CSA same for all three of adder cells. The analysis shows that the CSA using FZF logic is better in terms of power consumption and Power Delay Product (PDP) for all three FA cells however BEC based CSA proves to be better in terms of number of transistors used to implement the overall circuit. All the designs are implemented 1.8Volt power supply and 180nm CMOS process technology in Cadence Virtuoso environment.**

Keywords— MUX free CSA; First Zero Finding Logic; BEC; Carry Select Adder; 8T FA; 10T FA.

I. INTRODUCTION

In recent years a large amount of the research effort has been given to improve the system architectures as a whole such as ALU, FIR Filters, FFT implementation etc. However the backbone of a digital system is an adder block. Thus improvement of the adder block will lead to the improvement of the system as a whole without any change in the architecture of the system[1].This work provides a detailed analysis of the MUX free architecture of CSA [1,2] by making use of 28T [3], 10T[4] and 8T[5,6] adder. In the current VLSI industry optimization of both power and area are of prime importance since the demand of the consumers is not only restricted to smaller size of the devices but also higher battery life. In order to achieve such a design specification high speed architectures are to be considered one such architecture is CSA. The CSA is used in many computational systems to alleviate the problem of carry propagation delay by independent generating multiple carries and then select a carry to generate the sum[7]. However, due to the use of an extra Ripple Carry Adder (RCA) as the second stage and ultimately a final stage MUX the area consumed by such a CSA design is very huge, thus not only occupies a large area but also increases the power dissipation of the overall circuit, which can be a point of concern so as to make a device more and more portable. Hence in order to avoid the extra area and power consumption by the CSA an intelligent design scheme was given in[2] which gives the idea of using FZF logic circuit to eliminate the second stage RCA and final stage MUX in a traditional CSA design for front end implementation.

This paper is organized as follows, in section II, we explain the architecture of CSA using BEC logic, in section III architecture of CSA using FZF logic, in section IV Implementation of optimized FA cell, in section V Simulation and result analysis, in section V simulation and result analysis and in section VI give conclusion.

II. ARCHITECTURE OF CSA USING BEC LOGIC

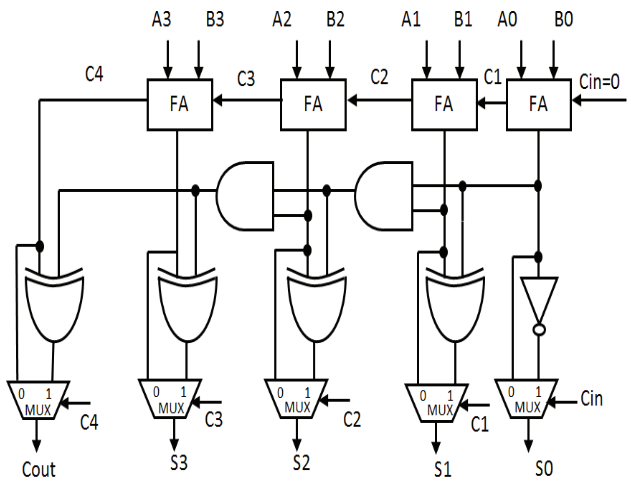

Fig. 1. Architecture of 4-Bit CSA using BEC logic

First, a traditional CSA will consist of the following major blocks that are first stage RCA, second stage RCA and final stage multiplexers for the final selection of the sum bit either for input carry being 0 or 1. In [1,2] a unique design is given that gives implementation of CSA with elimination of the second stage RCA. It uses a BEC logic block to perform the operation provided by the RCA as in Fig 1. When analyzed the second stage of a CSA is nothing but a RCA with input carry as 1, thus any circuit that gives add one operation can be placed in place of the second stage RCA to achieve the desired operation. The operation is achieved by using BEC logic.

A BEC is a combination of XOR gates in conjugation with AND gates such that each and gate acts as an internal carry generator circuit that generates the carry of the two

2015 International Conference on Advances in
Computers, Communication and Electronic Engineering
March 16-18, 2015
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Comparative Analysis Of Full Adder Cells in Nano-scale For Cascaded Applications

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Abstract

This paper focuses on the different designs of an Adder cell with an aim of finding an Adder cell from the literature which can be used for the future VLSI application. To ensure this all the designs have been implemented in Cadence Virtuoso 90nm Technology with least possible size of transistors available. A critical parameter in identifying circuits suitable for VLSI applications is that the implementation area and power dissipation must be as small as possible, thus in this paper we are trying to compare different possible design of an adder cell ranging from the most stable 28 transistor(28T) adder cell to a low area 8 transistor(8T) adder cell. All the designs have been compared for their area, power dissipation, delay and PDP, so as to choose the more reliable adder cell for cascaded VLSI applications.

"Keywords: Low Arear Full Adder; Nano Scale Adder;Lower Transistor Count;Threshold loss ;cascaded logic"

1. Introduction

In recent years a good number of researchers have focused their work for the optimization of system architectures such as that of a Filter, multipliers, MAC units etc. This methodology of optimization includes a huge amount of theoretical calculations and improvisations in the logic used to implement the architecture, so as to develop a new architecture that can prove to be better than the existing architecture. A simpler method to optimize any logic circuit can be to identify a base cell that can be repeated to form the complete architectural design of a system. For systems like multipliers and others the base cell that is in general recursively used is the Full Adder Cell. Thus optimization of a Full Adder Cell will lead to the optimization of the system as a whole while all the efforts are focused on optimizing a single unit out of the whole architecture i.e the Full Adder Cell.

Realizing the significance of a Full Adder Cell we have gone through the literature and identified a wide range of versatility in the design and also in the number of transistors used to implement each design. Some of the promising designs of Full Adder Cells have been implemented and compared in this paper. However a peculiar feature of reducing the area by reducing the number of transistors being used to implement the Adder cell is that the driving capability is also expected to vary as there is a serious degradation in the output voltage swings than the expected full swing voltage values be less as compared to the reference design of a Full Adder cell. Thus the cells given in this paper have been compared on the basis of amount of the degradation attained in the output logic level for respective input combinations, power consumption and delay. As we tend to reduce the number of the transistors used to implement an adder cell starting from the fully symmetrical design of a 28T Adder cell R. Zimmermann et al., 1997 and going down to least possible 8T Adder cell Fayed et al., 2001 there is a variation in the amount of the degradation levels attained in either Sum or Carry output or-else both, which ultimately restricts the driving capability of respective Full Adder Cell. Each adder cell has been somewhat modified by varying the W/L ratio of the transistors used in the design of that particular adder cell so as to attain some acceptable logic levels of Sum and Carry outputs, which help in proper driving of the next stages of the circuit.

ISBN: 978-93-8222288-54-1

Comparative Analysis of Carry Select Adder using 8T and 10T Full Adder Cells

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Abstract—**This paper present a comparison between the design of the 8T adder based Carry Select Adder (CSA) and 10T adder based CSA. Using both the designs of adders 4-bit CSA architecture has been developed and compared with the 28T adder 4-bit CSA. The 10T CSA design has reduced delay, power and area as compared with the 28T CSA with a slight tradeoff for area as compared to 8T CSA. The analysis shows that the 10T CSA is better than both 8T adder based CSA and 28T CSA. This work evaluates the performance of the 10T CSA design in terms of power, delay and area using 180nm CMOS process technology Cadence Virtuoso tool and Spectre simulator.**

***Index Terms*— Carry Select Adder (CSLA); Low power; Binary Excess -1 Converter (BEC), 10 Transistor adder.**

I. Introduction

In recent years a large amount of the research effort has been given to improve the system architectures as a whole such as ALU, FIR Filters, FFT implementation etc., however the backbone of a digital system is a adder block. Thus improvement of the adder block will lead to the improvement of the system as a whole without any change in the architecture of the system. This works provides a detailed analysis of the already existing architecture of CSA [1] by making use of 28T [2], 8T [3], and 10T [4] adder. In the current VLSI industry optimization of both power and speed are of prime importance since the demand of the consumers is not only restricted to smaller size of the devices but also higher speeds with longer battery life. In order to achieve such a design specification high speed architectures are to be considered one such architecture is CSA than provides a good speed and lower power consumption with area trade off. The CSA is used in many computational systems to alleviate the problem of carry propagation delay by independent generating multiple carries and then select a carry to generate the sum. However, the CSA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1, then the final sum and carry are selected by the multiplexers (MUX) [5].

This paper is organized as follows, in section II, we examine the existing CSA with BEC using 28T, in section III Implementation of CSA using 8T, in section IV Implementation of CSA using 10T, section V simulation and result analysis are discussed. The last section includes conclusion and references.

II. Existing CSA With BEC Using 28T Full Adder Cell

The Existing work gives the implementation of the CSLA using 28T [2] 1- bit full adder. For each full adder block in first level RCA block with Cin=0, and in second level Binary Excess Converter (BEC) is used instead of RCA with Cin=1 in regular CSA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. Hence reduces the area and power consumption of the regular CSLA to replace the n-bit RCA by an n+1-bit BEC. A structure and the function table of a 4-bit BEC are shown in Fig.1 and Table I respectively [6].

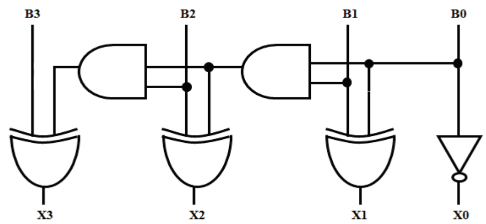

Fig.1 4-bit Binary Excess Converter

One of the biggest advantages of using this BEC logic is that when large amount of the bits are sent to CSA for addition BEC logic usage saves a very large amount of area as compared to RCA which is used in the conventional CSA. The equation (1) shows Boolean expression of 4-bit Binary Excess Converter [1].

$$\begin{aligned} X0 &= \overline{B0} \\ X1 &= B0 \oplus B1 \\ X2 &= B2 \oplus (B0 \,\&\, B1) \\ X3 &= B3 \oplus (B0 \,\&\, B1 \,\&\, B2) \end{aligned} \quad (1)$$

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978-1-4799-3357-0

A Review Paper On 3-T Xor Cells And 8-T Adder Design in Cadence 180nm

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***Abstract*— The paper gives a review of already existing 3-T XOR cells and provides an optimized value of (W/L) on the basis of simulation results obtained, so as to improve the threshold loss problems present in the existing designs of 3-T XOR cells thus helping improve the driving capability, however the driving capability is not sufficient for large circuits like multipliers, hence has a scope for further improvement. Using the best improved version of 3-T XOR cell a Full Adder Circuits is designed. All the basic circuits and their improved versions have been implemented in Cadence Virtuoso for 180nm technology and 1.8v sources.**

Keywords—*3T-XOR, 8-T Adder, Threshold loss problem*

1. INTRODUCTION

Various efforts have been made in the past to optimize arithmetic circuits in terms of their speed, implementation area, power consumption and so on. However the path chosen to achieve this aim may vary from one designer to another. One such way to optimize any arithmetic circuit is to optimize its basic building blocks to obtain optimized speed, area and power consumption for the overall circuit.

Adder being the basic building block of an arithmetic circuits such as multiplier, MAC unit, ALU, hence its optimization can lead to the optimization of a very large number of arithmetic circuits as a whole, hence design of low power, high speed adder has become one of the most essential and important research problems[7-9] . However the heart of an adder circuit is XOR gate. Therefore an optimized XOR gate has to be a prior matter of concern for a designer before designing a Full Adder Cell. Analyzing the literature available on XOR gate a wide number of designs have been developed to attain the desired function of an XOR gate. Ranging from a 12-T XOR gate in [1] the number of transistors, speed, area on chip and power consumption to implement the XOR function have been improved up to an acceptable level of satisfaction by designing 3-T XOR gate in [2-3-4]. However as the number of transistors decreases the threshold loss problems seem to creep in to the picture, due to which it becomes very difficult to cascade such a gate where the output suffers threshold loss problem. In order to explain the amount of threshold loss problem, all outputs are represented in the form of voltage values for 1 and 0, which ideally must be 1.8v and 0v respectively. Thus all the output values are shown in terms of voltage values rather than logic values. Rest of the paper is distributed in following sections: section 2 is simulation results of designs given in previous literature, section 3 is improved w/l selected design and its simulation results, section 4 is improved 8-T adder, section 5 is conclusion and section 6 is references.

2. SIMULATION RESULTS OF PREVIOUS LITERATURE

Three basic designs for 3T-XOR gate given in [1-2-3] have been designed and analyzed for their performance using cadence virtuoso 180nm technology. Each of the design will be analyzed and compared with each other on the basic of output logic value voltages and average power. More-over in this paper we have chosen two types of input combination sequence one is as sequence 1{00, 01, 10, 11} and the other one is sequence 2{11, 10, 01, 00}. The output response of the circuit is recorded in tables with average output logic voltage values for each of the input combination for all circuits.

A. **XOR Cell I,** is implemented using the design in [3] which is shown in figure 1 with respective waveforms for both sequences in figure 1a and 1b.

All the w (width) in w/l ratios are calculated with respect to the technology used that is 180nm thus the values for w used for the design in [3] are 400nm,900nm and 400nm for PM0,PM1 and NM0 respectively. However the ratios given in the paper are 1/1 for NM0 but it is taken to be greater than 2/1 because of design constrains. This paper uses two types of sequences so as to analyses the effect of the charge storage on the output waveform of the XOR cell. Since ideally no charge storage is expected but practically it is there in the MOS devices. The output response observed is given in table 1 for two types of input sequence and the effect can be analyzed as:

For sequence 1 the circuit supplies a very weak logic 1 for {10} combination, where as rest of the logic voltages can somehow be accepted. The Average power of the circuit is 48.62E-6.

For sequence 2 the circuit supplies a very weak logic 0 for {00}, where as rest of logic values can somehow be accepted. The average power of the circuit is 49.56E-6.

978-1-4799-3759-2/14/$31.00©2014 IEEE

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