OFFICE OF THE DEAN ENGINEERING

SCHOOL OF ENGINEERING

UNIVERSITY OF KASHMIR (NAAC ACCREDITED A+)

F (Major-Exam-Oct/Nov-ECE) DSE/KU/21
Dated: 10th January 2021

(REVISED) Online Examination Schedule of 3rd Semester (Backlog) Batch 2017 only
B.Tech. Electronics and Communication Engineering

Date	3rd Semester (2017 batch only)		
	2:30 p.m. to 3:00 p.m.		
13/01/2021	MTH3117B	Engineering Mathematics – III	
14/01/2021	ECE3217B	Network Analysis and Synthesis	
15/01/2021	ECE3317B	Analog Electronic Circuits -1	
16/01/2021	ECE3417B	Signals & Systems	
17/01/2021	ECE3517B	Material Science	
Lab Examination Schedule			
	Lab		Time (IOT)
19/01/2021	Network analysis and synthesis Lab		10:30 a.m.
	Analog Electronic Circuits lab		12:00 p.m.
20/01/2021	EDA Tools Lab		10:30 a.m.

Note:

1. Only those students will be allowed to appear in the Examination that submit their Examination form and fees before start of examination.

Prof. S. M. A. Andrabi
(Dean School of Engineering)

Copy to

1. Controller Examination, University of Kashmir
2. Head/Coordinators, Institute of Technology
3. Website